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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,042	03/19/2001	Li T. Wang	062891.0520	1363

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,042	WANG, LI T.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1-3,8-10 and 15* is/are rejected.

7)☒ Claim(s) *4-7,11-14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, 8, 10, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukagoshi et al. U.S Patent 6,072,333.

Regarding claims 1 and 15, in column 1 lines 7-32, Tsukagoshi et al. discusses a tristate output circuit of a prior art in figure 3. The tristate output circuit comprises a control unit 36 consisting of transmission gates 31 and 32, a P-channel MOS transistor 34 and an N-channel MOS transistor 35, amplifier stages 37 and 38, and an output stage 312, which has a P-channel MOS transistor 39, and an N-channel MOS transistor 310.

- in1 provides a first data signal, corresponding to the claimed providing a first data signal.
- in2 provides a second data signal, corresponding to the claimed providing a second data signal.
- The terminal 313 is set to "L" so that transmission gates 31 and 32 are closed. The P-channel MOS transistor 34 and the N-channel MOS transistor 35 are turned on. As a result, both the P-channel MOS transistor 39 and the N-channel MOS transistor 310 are turned off, and the output terminal 311 is

set to be floating, thereby attaining a high impedance, see column 1 lines 45-52. Tsukagoshi et al. does not expressly disclose in1 data signal is a logical one. However, as discussed above, as a result of P-channel MOS transistor 39 being turned off, it would have been obvious for one of ordinary skill in the art at that in1 produces a zero voltage, which is equivalent to a logical 0. Therefore, output terminal 311 has a first state output.

- The terminal 313 is set to "H" so that the transmission gates 31 and 32 are opened. The P-channel MOS transistor 34 and the N-channel MOS transistor 35 are turned off. Signals are applied to input terminals in1 and in2 of the transmission gates 31 and 32, respectively. The signals at the input terminals in1 and in2 are amplified by the amplified stages 37 and 38, and then applied to the P-channel MOS transistor 39 and the N-channel MOS transistor 310, respectively. These transistors are complementarily turned ON and OFF so that the output terminal 311 is set to be "H" or "L". Because Tsukagoshi et al. does not discuss any specific combination of ON and OFF in the prior art to generate logical "L" and "H" at the output terminal 311, one person of average skill in the art can arbitrarily assign a logic "L" to output terminal 311 when P-channel MOS transistor 39 is turned on while the N-channel MOS transistor 310 are turned off. As a result of P-channel MOS transistor 39 being turned on, the first data signal is equivalent to a logical one and the logic "L" generated at the output terminal 311 corresponds to a second state as claimed in the instant application.

- Tsukagoshi et al. does not disclose in the prior art the case when both P-channel MOS transistor 39 and the N-channel MOS transistor 310 are turned on. Nevertheless, when both P-channel MOS transistor 39 and the N-channel MOS transistor 310 are turned on, it will be appreciated that the voltage level at the output terminal 311 will be higher than the case when the transistors are complementarily turned ON and OFF. Because of a higher voltage also corresponding to a logical "H", it would have been obvious for one of ordinary skill in the art at the time the invention was made that the tristate output circuit in figure 3 can be modified to generate a logical "H" when both P-channel MOS transistor 39 and the N-channel MOS transistor 310 are turned on. The logical "H" at the output terminal corresponding to a third state as claimed in the instant application. When the P-channel MOS transistor 39 and the N-channel MOS transistor 310 are turned on, the first data signal and the second data signal are applied to the transistors 39 and 310, equivalent to logical "1" as claimed in the instant application. As further described in column 2 lines 14-27, a tristate output circuit is configured so that, when clock signal consisting two states of "H" and "L" is to be generated as required, an output of an appropriate duty is obtained. The motivation is that there are no specific teachings of generating logic "L" and "H" at the output terminal 313.

Regarding claims 3 and 10, as discussed in claim 1, when the P-channel MOS transistor 39 is turned on and the N-channel MOS transistor 310 is turned off to

generate a second state, the N-channel MOS transistor 310 is in an open drain state, typically considered logic "0" as appreciated by a person of average skill in the art. As a result of that, the amplifier 38 coupled to the output terminal 311 is placed into an open drain state, corresponding to the claimed limitation.

Regarding claim 8, claim 8 and claim 1 have similar scope. Claim 8 is rejected on the same ground as for claim 1. Furthermore, referring to figure 3, amplifier 37 receives a first data signal in1, and corresponds to the claimed first amplifier. Amplifier 38 receives a second data signal in2, and corresponds to the claimed second amplifier.

2. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukagoshi et al. U.S Patent 6,072,333 as applied to claim 1 above and further in view of Trimberger U.S. Patent 5,973,506.

Regarding claims 2 and 9, Tsukagoshi et al. does not expressly disclose the claimed feature. Nevertheless, Trimberger discusses a prior art in figure 8 wherein tristate buffers 801, 802, 803 are coupled to line 800 employing a pull-up resistor 813. Trimberger further discusses that the pull-up resistor 813 can be implemented with an NMOS transistor or with a PMOS transistor, see column 8 lines 18-28. Referring back to figure 3 of Tsukagoshi et al. invention, the P-channel MOS transistor 34 is coupled to the first data signal line. Because a pull-up resistor 813 can be implemented with an NMOS transistor or with a PMOS transistor as recited above, it would have been obvious for one of ordinary skill in the art that the P-channel MOS transistor 34 performs

as an equivalent pull-up resistor. As discussed in claim 1 above, in the first state, the P-channel MOS transistor 34 is turned on and the P-channel MOS transistor 39 is turned off, as result of that, the voltage of data line from the first voltage level is pulling towards a zero voltage level as claimed in the instant application.

Allowable Subject Matter

3. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 4, claim 4 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "wherein driving the release data line to a third state comprises placing an output of a first amplifier coupled to the data line into an open drain state".

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 5, claim 5 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "driving the release data line to a third state comprises placing an output of a first amplifier coupled to the data line into an open drain state".

5. Claims 6 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 6 and 13, claims 6 and 13 are allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "the first amplifier comprises an open drain Gunning Tranceiver Logic (GTL) buffer" and "the second amplifier comprises an Stub Series Terminated Logic (SSTL) output driver".

6. Claims 7, 14 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 7, 14 and 18, claims 7, 14 and 18 are allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "the first state comprises an approximate 0.4 voltage level on the data line" and "the second state comprises an approximate 1.2 voltage level on the data line" and "the third state comprises an approximate 2.3 voltage level on the data line".

7. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 11, claim 11 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "wherein the first amplifier establishes an open drain state to release the data line so that the second amplifier can drive the data line to the third state".

8. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 12, claim 12 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "wherein the first amplifier establishes an open drain state to release the data line so that the second amplifier can drive the data line to the third state".

9. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 16, claim 16 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "means for driving the released data line to a third state comprises: means for placing an output of a coupled to the data line into an open drain state".

10. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 17, claim 17 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose "the means for driving a data line comprises an open drain Gunning Tranceiver Logic (GTL) buffer" and "the means for driving the released data line comprises a Stub Series Terminated Logic (SSTL) output driver".

11. Claims 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 19, claim 19 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose a communication server comprising all elements as set forth in the claimed invention.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Krishnamurthy et al. U.S. Patent 5,986,473 discloses "Differential, Mixed Swing, Tristate Driver Circuit for High Performance and Low Power On-Chip Interconnects".

Fletcher et al. U.S. Patent 6,320,441 B1 discloses "I/O Transceiver Having A Pulsed Latch Receiver Circuit".

Engles et al. U.S. Patent 5,867,053 discloses "Multiplexed Output Circuit And Method Of Operation Thereof".

Boudry et al. U.S. Patent 6,470,054 B1 discloses "Bidirectional Two-Way CMOS Link Tailored For Reception and Transmission".

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

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